RESET CURRENT DELIVERY IN NON-VOLATILE RANDOM ACCESS MEMORY

FIELD

[0001] Embodiments of the present disclosure generally relate to the field of integrated circuits, and more particularly, to set and reset operation in non-volatile random access memory (NVRAM) devices, such as phase change memory devices.

BACKGROUND

[0002] Phase change memory (PCM) technology such as multi-stack cross-point PCM is a promising alternative to other non-volatile (NV) memory technology, commonly known as non-volatile random access memory (NVRAM). Presently, reset current delivery has been a challenge in PCM memory technology due to high cell current requirement and high word line and bit line path resistance. The current mirror architecture used for reset current delivery has limited reset current delivery capability because the negative power supply of the reset current mirror may typically be set to be the inhibit voltage of the cross-point array, in order to avoid false selection of memory cells in the cross point array.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

[0004] FIG. **1** is an example circuitry of an NVRAM device, such as a PCM device, in accordance with some embodiments.

[0005] FIG. **2** is an example diagram illustrating a reset operation of an NVRAM (e.g., PCM) device, in accordance with some embodiments.

[0006] FIG. **3** is an example process flow diagram of a method **300** for performing a reset operation of an NVRAM (e.g., PCM) device, in accordance with some embodiments.

[0007] FIG. **4** is an example system that includes an NVRAM (e.g., PCM) device in accordance with various embodiments described herein.

DETAILED DESCRIPTION

[0008] In the following detailed description, reference is made to the accompanying drawings that form a part hereof wherein like numerals designate like parts throughout, and in which is shown by way of illustration embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of embodiments is defined by the appended claims and their equivalents.

[0009] Techniques for providing a reset current to an NVRAM device, such as a PCM device, are discussed herein. In one instance, the apparatus may comprise an NVRAM (e.g., PCM) device; a selection mirror circuit coupled with the NVRAM device to apply a selection mirror voltage to the NVRAM device, to select a memory cell of the NVRAM device; and a reset mirror circuit coupled with the NVRAM device to apply a reset mirror voltage to the memory cell of the NVRAM device, subsequent to the application of the selection mirror voltage, to reset the memory cell. The reset mirror voltage may be lower than the selection mirror voltage, to facilitate delivery of a reset current above a current threshold to the memory cell.

[0010] Various operations are described as multiple discrete operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order than the described embodiment. Various additional operations may be performed and/or described operations may be omitted in additional embodiments.

[0011] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

[0012] The description may use the phrases "in an embodiment," or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The term "coupled" may refer to a direct connection, an indirect connection, or an indirect communication.

[0013] As used herein, the term "module" may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, state machine, and/or other suitable components that provide the described functionality.

[0014] FIG. **1** schematically illustrates example apparatus **100** of an NVRAM device, such as a PCM device in accordance with some embodiments. According to various embodiments, the apparatus **100** may include one or more memory cells (hereinafter "memory cells **102**"), which may be configured in an array as shown. The memory cells **102** may include, for example, a phase change material such as a chalcogenide glass that can be switched between crystalline and amorphous states with the application of heat produced by an electric current. The state (e.g., crystalline/amorphous) of the phase change material may correspond with a logical value (e.g., 1 or 0) of the memory cells **102**. The apparatus **100** may be part of a phase change memory and switch (PCMS) device in some embodiments. The memory cells **102** may include a switch such as, for example, an ovonic threshold switch (OTS) configured for use in selection/programming operations of the memory cells **102**. In other embodiments, the apparatus **100** may be part of other suitable types of memory devices. Regardless, as will be described in more detail below, the apparatus **100** may be incorporated with the reset current delivery technology of the present disclosure to facilitate delivery of a reset current above a current threshold to the memory cells.